



Wirelength driven floorplacement for FPGA-based partial reconfigurable systems

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Rationale and Innovation



- Problem statement
 - ▶ Given a reconfigurable architecture, find an on-chip position for each functional unit (FU)
- Innovative contribution: a *formalization* and an *approach* taking concurrently into account
 - ▶ Target Device Heterogeneity
 - ▶ Target Device reconfiguration capabilities
 - ▶ Inter-FU Communication
 - ▶ Inter-FU Wirelength



Outline



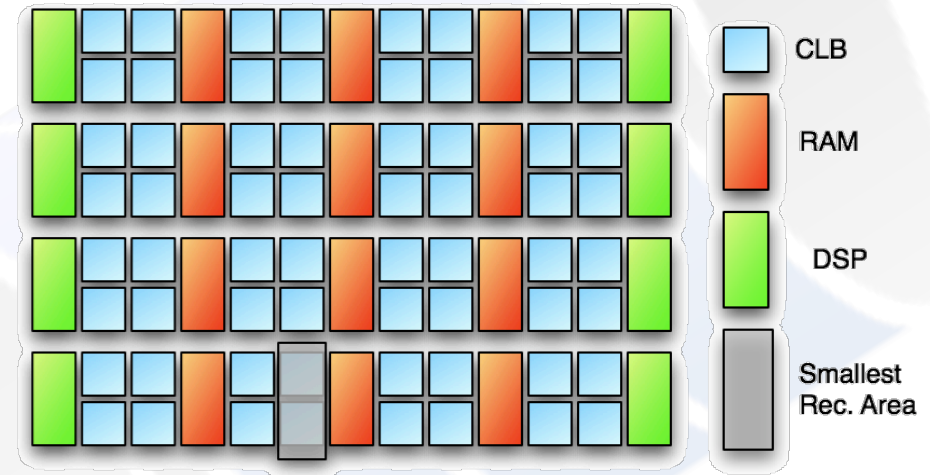
- Introduction and Useful Definitions
- Related Works
- Proposed Formalization & Area-Driven Approach
 - ▶ Wirelength-Driven Approach
- Results
- Conclusions and Future Work
- Question



Reconfigurable Architectures - I



- On FPGAs
 - ▶ Reconfigurable Devices
 - ▶ Heterogeneous
 - ▶ Reconfiguration Limits



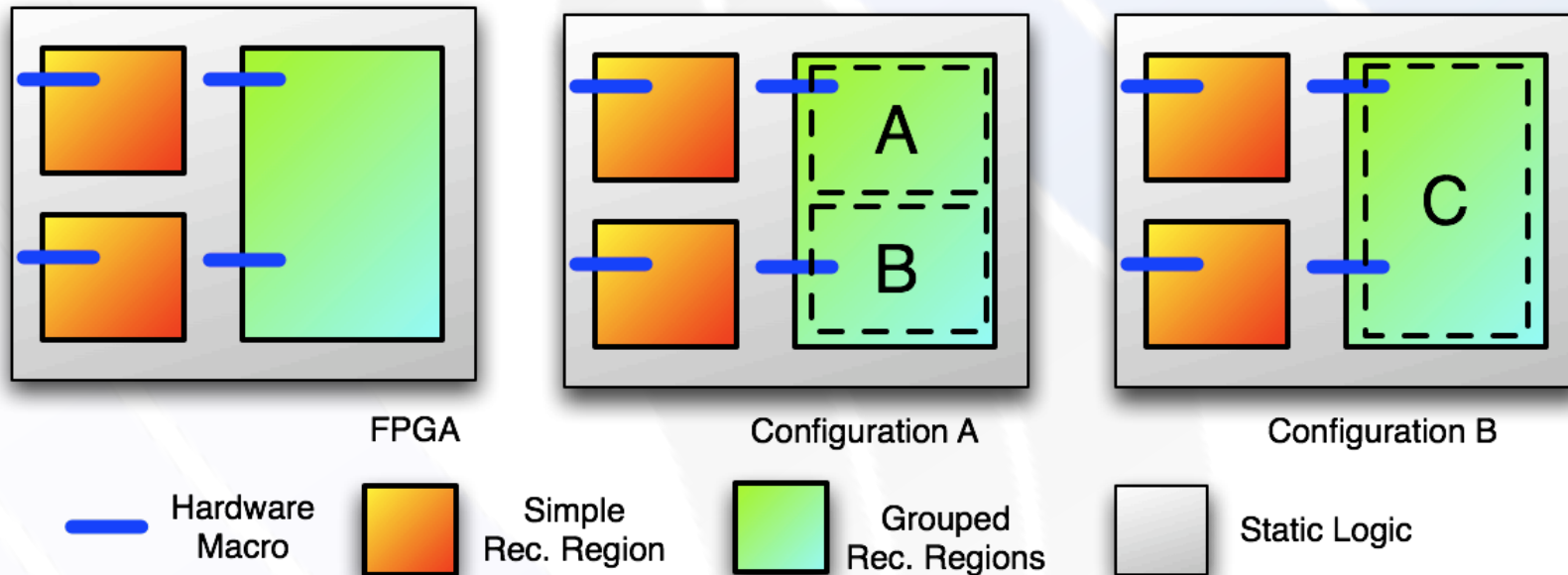
- Different types of Reconfigurable Architectures:
 - ▶ Total
 - ▶ Partial (Static)
 - ▶ Partial (Dynamic)



Definitions



- Reconfigurable Functional Unit (RFU)
 - ▶ A netlist obtained after post synthesis and technology mapping (i.e., before placement and routing)
- Reconfigurable Region (RR)





Related Works



Authors	Comm. Infrastructure	Resource Aware	Reconfiguration Aware	Device Limits Aware
Bazargan et al.	No	No	Yes	No
<i>Yuh et al.</i>	<i>Limited, w/ High Overhead</i>	<i>No</i>	<i>Yes</i>	<i>Yes</i>
Singhal et al.	No	No	Yes	No
Feng et al.	No	Yes	No	No



Proposed Problem Description

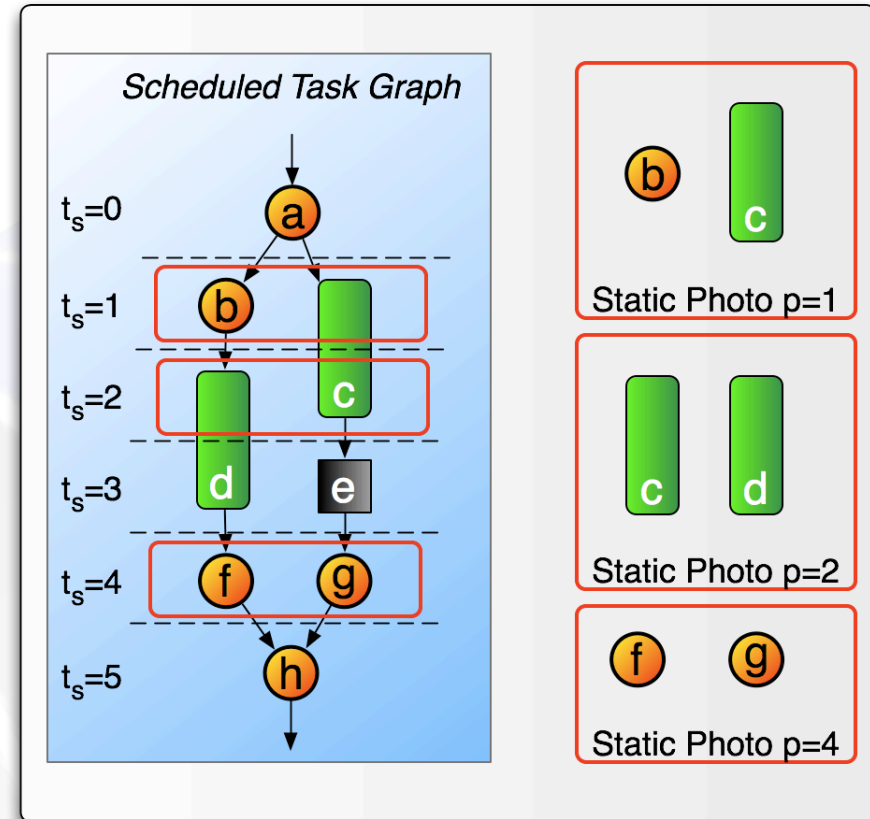


- Given an Application's Scheduled TG

- Define RRs
- For each task find
 - a suitable RR
 - a position inside RR

- Objective Function
 - Min. Fragmentation

- Constraints
 - Communication issues
 - Device limits



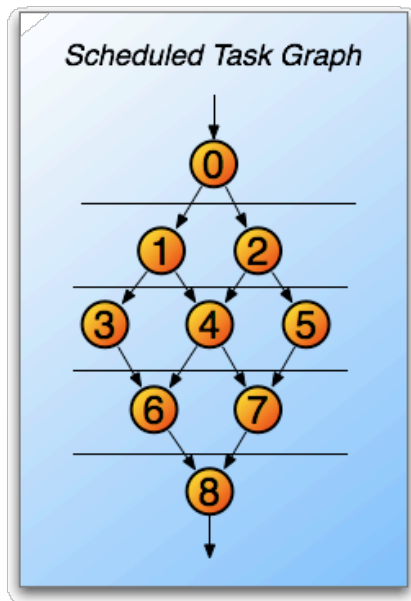
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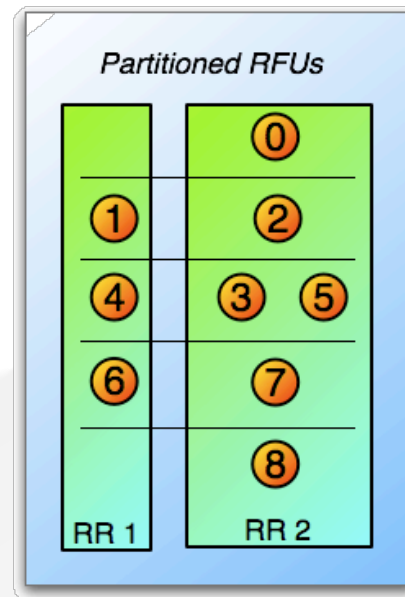
Proposed Approach: overview



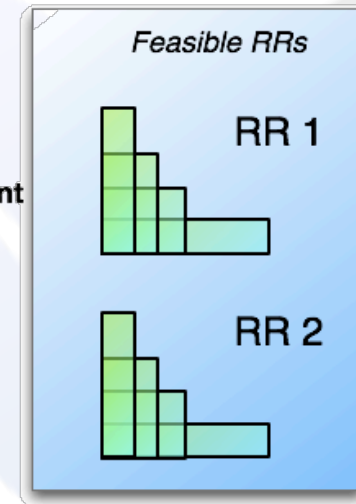
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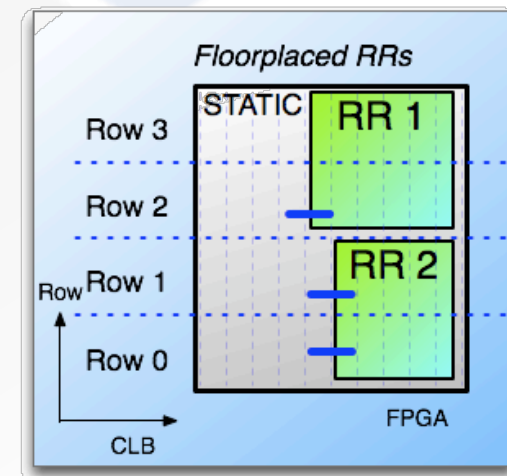
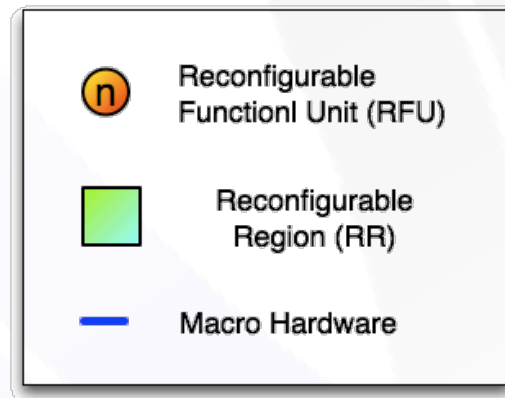
Partitioning into RRs



Temporal Floorplacement inside RRs



RRs Floorplacement





1st Algorithm: Partitioning into RR



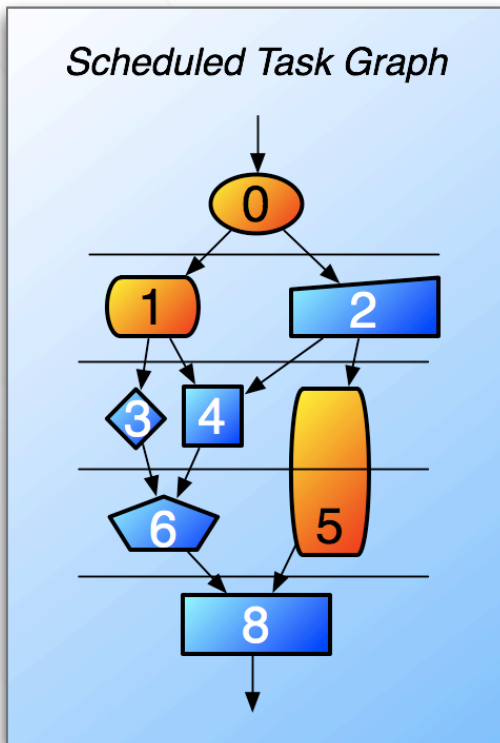
- **Aim:** identify the RRs and associate each RFU to one RR
- **How:** partitioning the TG minimizing resource requirement variance of the RRs (moving and swapping nodes)

$$\text{Var}(\rho_{n,p,t}) = \frac{1}{P} \sum_p (\rho_{n,p,t} - \overline{\rho_{n,p,t}})^2$$

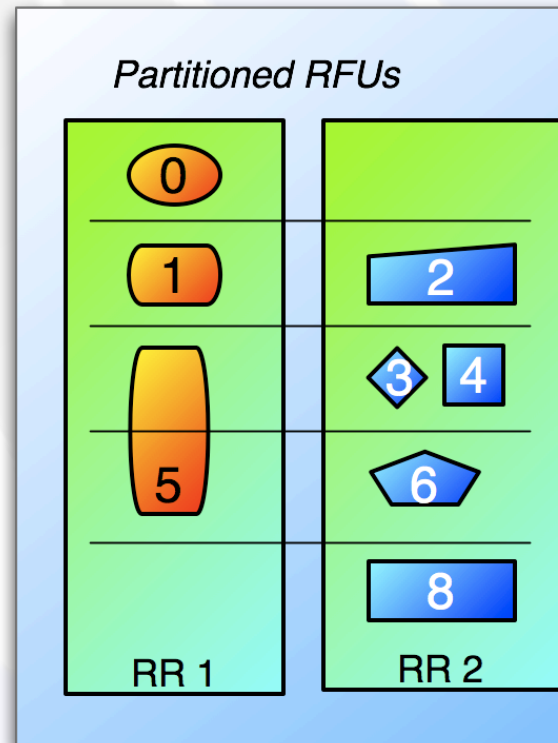
$\rho_{n,p,t}$

=

Resource of type t required by RFU n , at static photo p



Partitioning into RRs



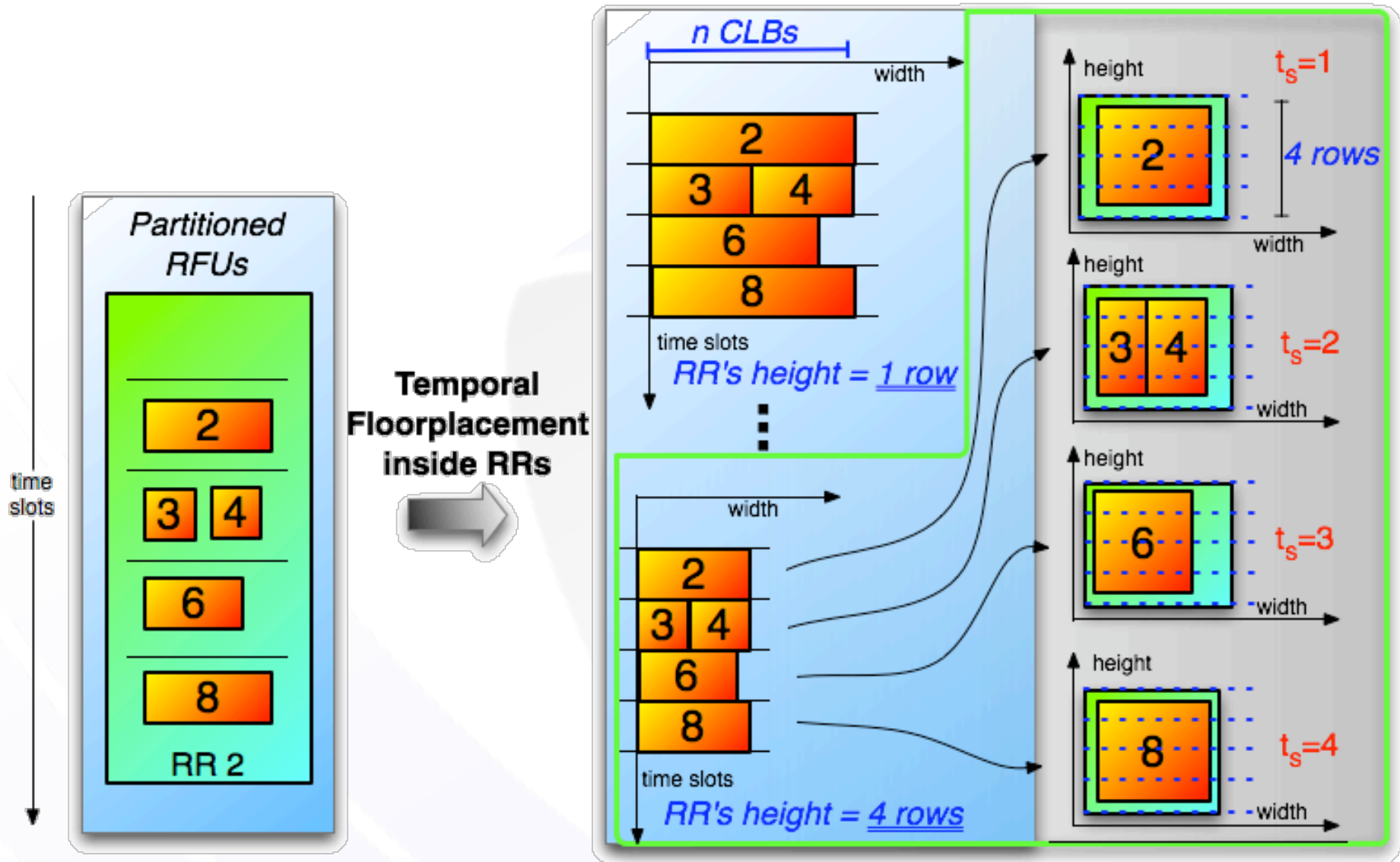
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2nd Algorithm: TFiRR



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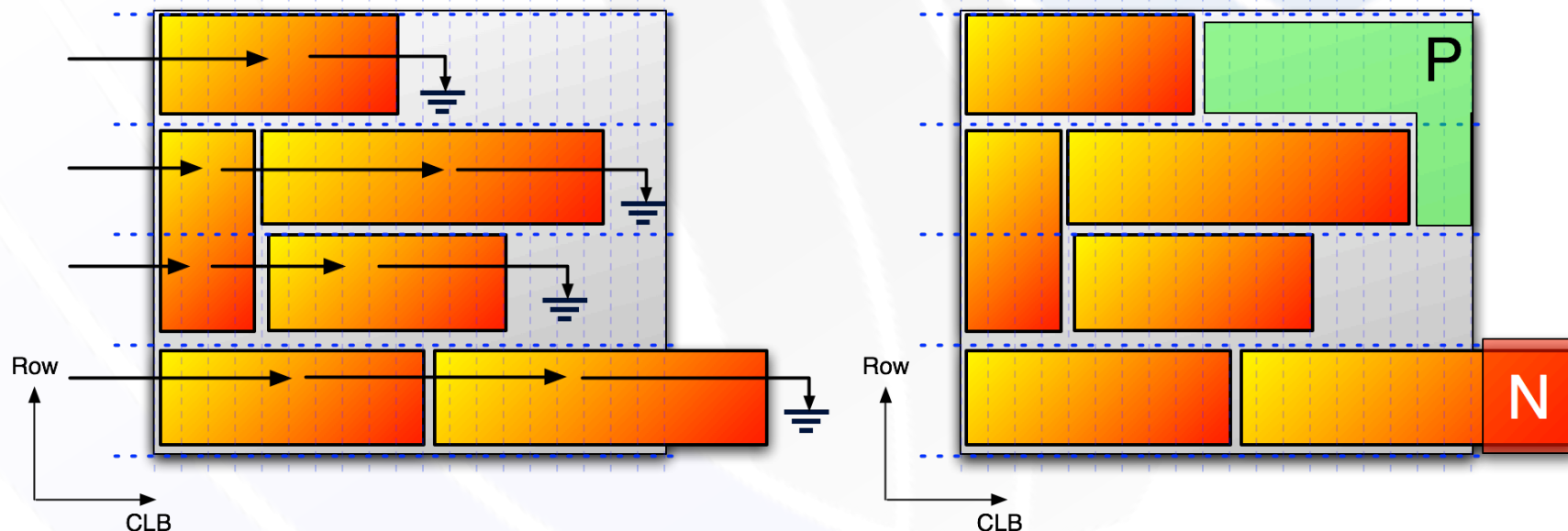




3rd Algorithm: RR floorplacement



- Simulated Annealing
 - ▶ Objective Function (positive iff floorplacement is feasible)
$$\Theta = P - M \cdot N$$
 - ▶ Data Structure
 - 4 Constraint Lists (one per row)
 - ▶ Moves: Swap, Move, Span, Un-Span

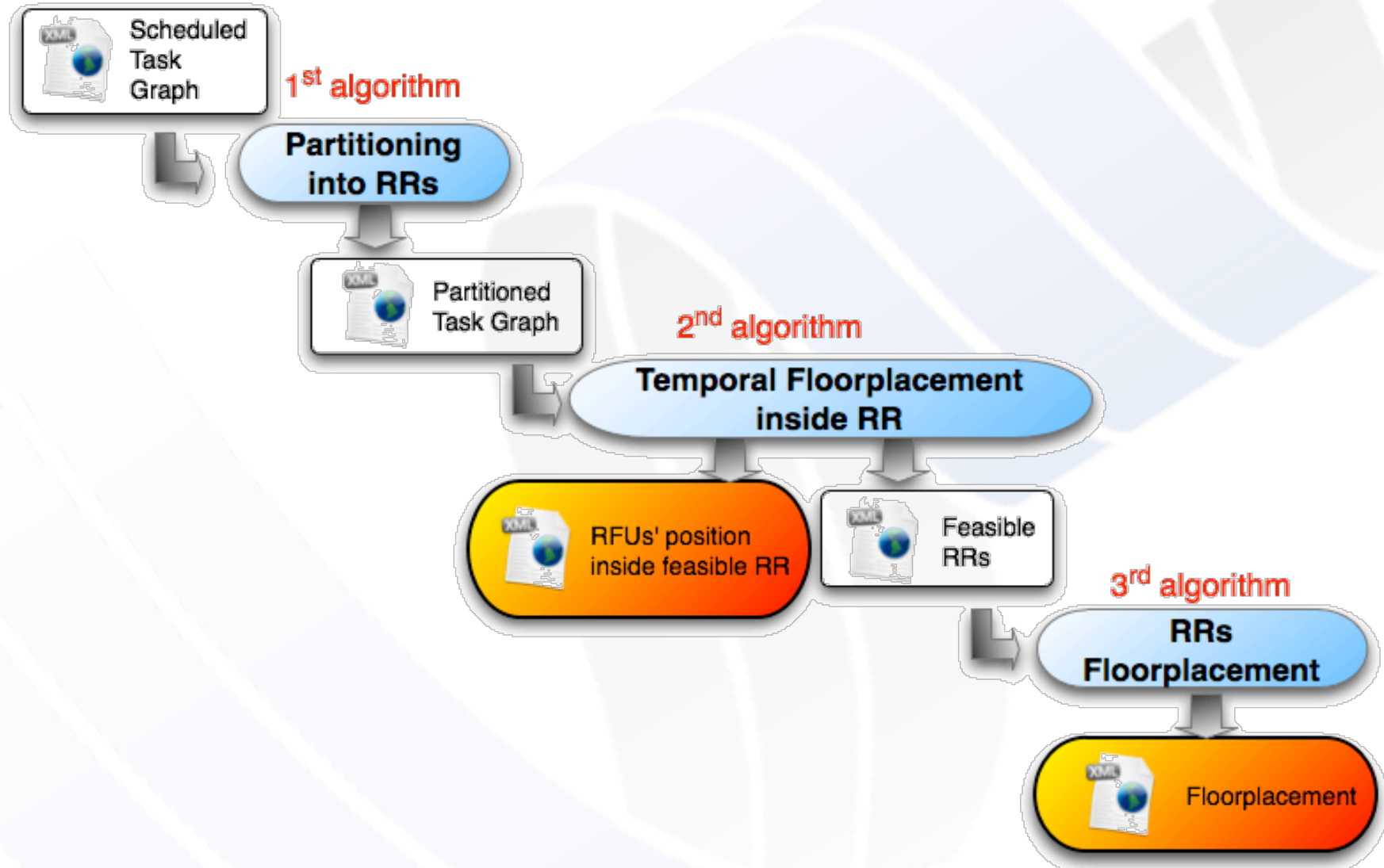




Implementation



- Three simulated annealers written in C++ STL



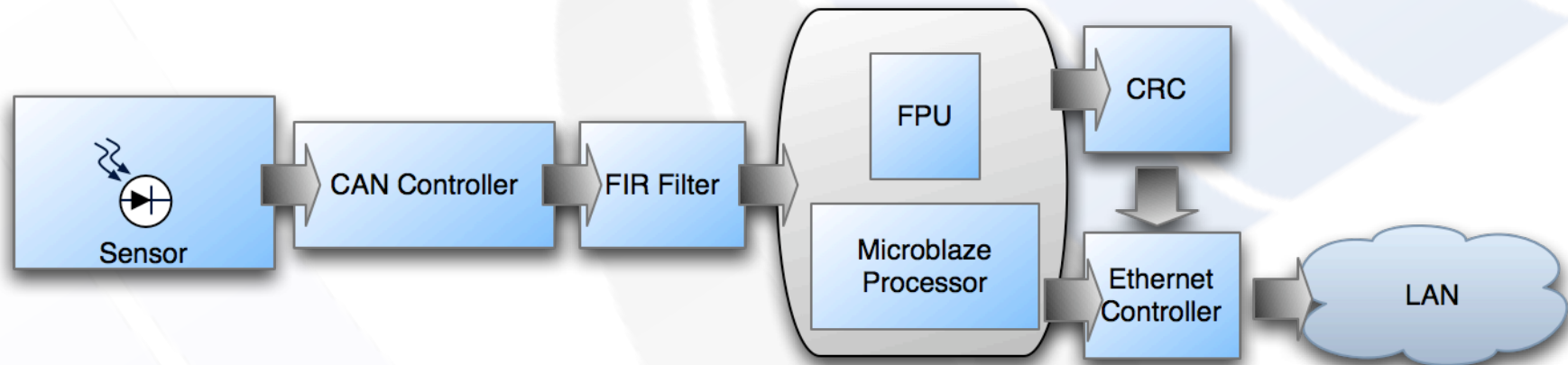
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Results - I: Case Study



- A Reconfigurable Architecture (for Biomedical Purpose) on XC5VLX30T
 1. Collecting data from sensor
 2. Elaborating them
 3. Sending to a host computer thorough the net



- Results w.r.t. the state of the art [*]:
 - ▶ 5% more chip area required
 - ▶ 2 OoM improved throughput communications

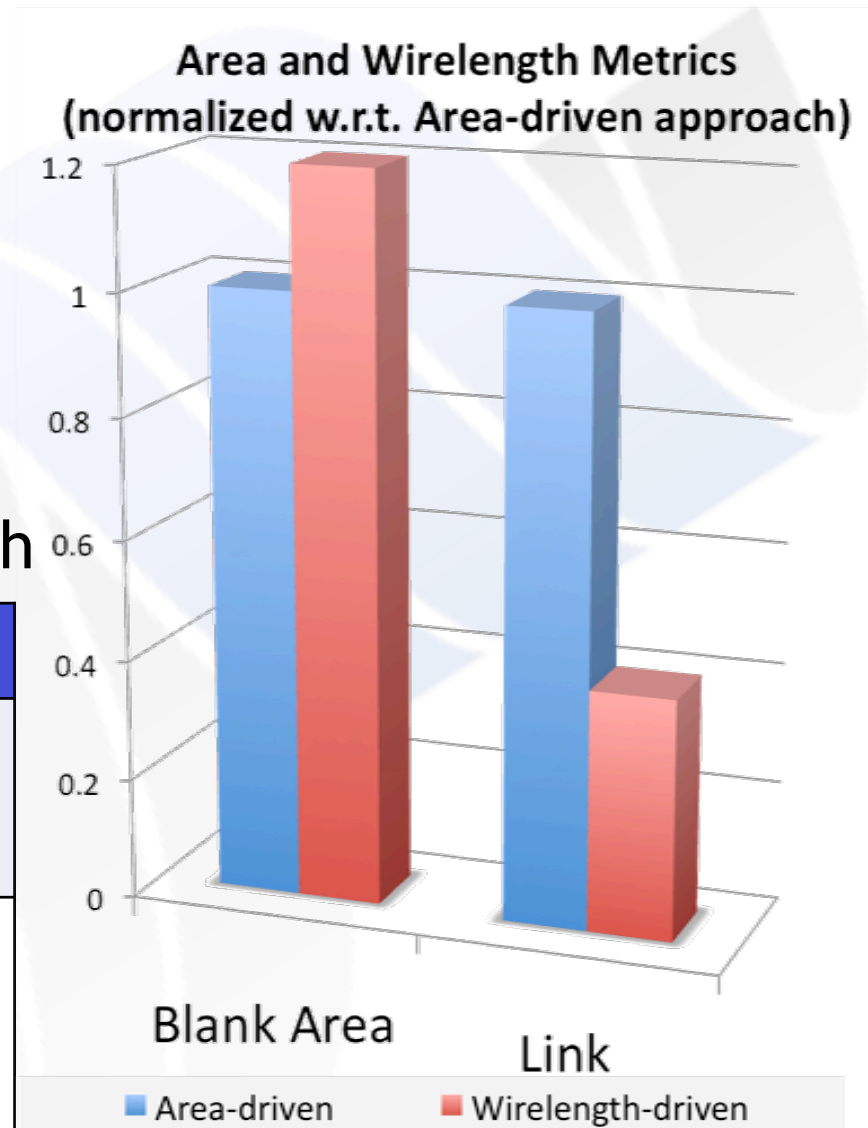


- Used Area

Metric	Variation/Value
Blank Area	(5,35)% of the final floorplacement

- Wirelength-driven Approach

Metric	Variation/Value
Links	(-90,0)% of the number of links required by a purely area-minimizing approach
External Wirelength	(-90,-30)% of the external wirelength given by a purely area-minimizing approach



Conclusions & Future Work



- ✓ An algorithm for the identification of area constraint for reconfigurable architectures has been introduced
- ✓ Novelties: taking into account
 - ▶ Target device heterogeneity
 - ▶ Target device reconfiguration capabilities
 - ▶ Communication issues
 - ▶ Inter-RFU wirelength
- Future work
 - ▶ partitioning with different metrics (e.g., Clock Domains)
 - ▶ consider non-periodic Resources
 - ▶ use the floorplacer as feedback for a scheduler