An Architectural Space Exploration Tool for Domain Specific Reconfigurable Computing

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Outline

- Motivation
- A domain-specific fabric
- Design space exploration case studies
- Automation of design space exploration
- Results
- Conclusions

Motivation

- ***Designing a complex SoC design requires the evaluation of many potential architectural options***
- ***Exploring the design space manually would be very time consuming and may not be feasible for complex designs***

One approach is…

- **To develop design space exploration tools**
  - **Allow application developers to explore architectural tradeoffs efficiently and reach solutions quickly**
  - **Consider the applications of interest that will run on the device**

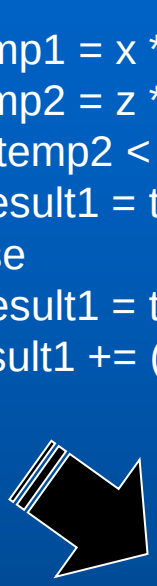
Signal and image processing applications

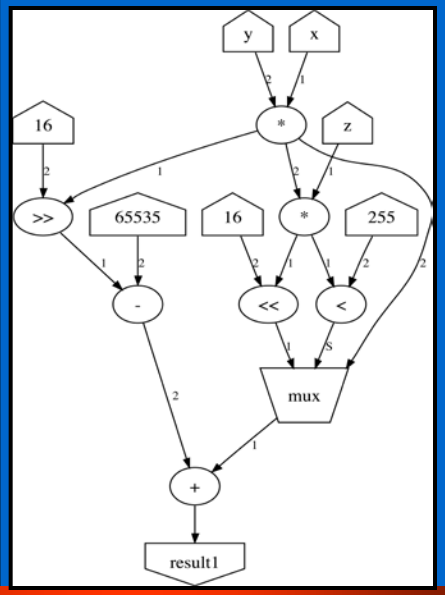
- **Core signal processing benchmarks from MediaBench benchmark suite**
- **Edge detection benchmarks from image processing domain**

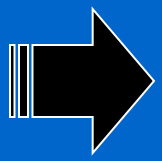


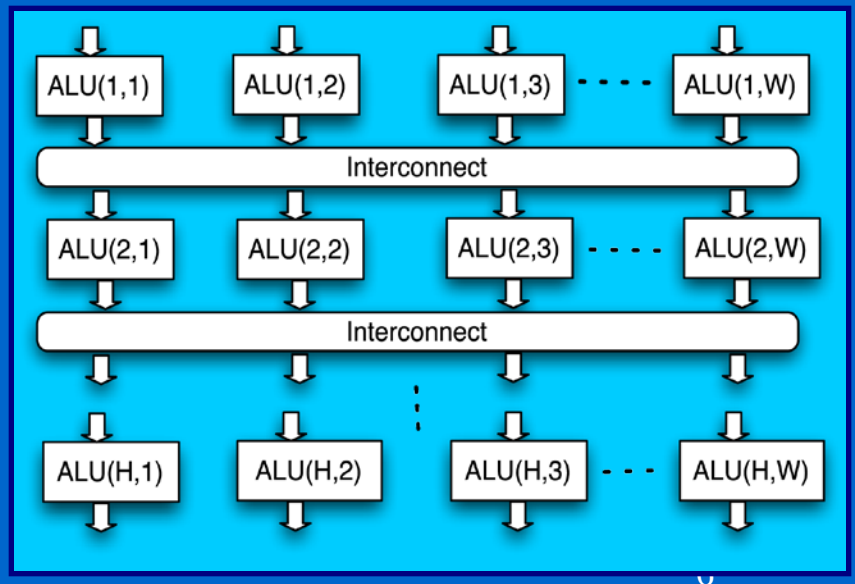
Mapping of a benchmark onto the fabric

```
temp1 = x * y;
temp2 = z *temp1;
if (temp2 < 255)
  result1 = temp2<<16 ;
else
  result1 = temp1;
result1 += (((temp1)>>16)-0xffff);
```



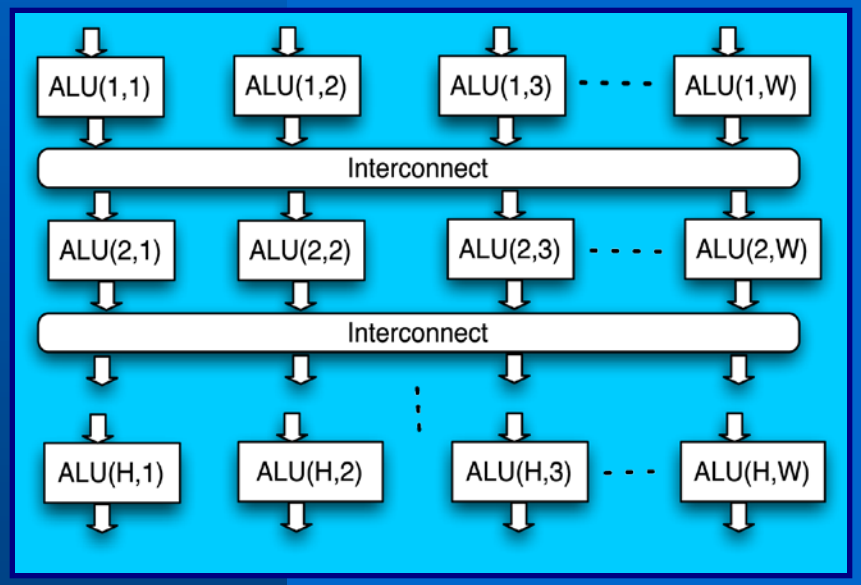






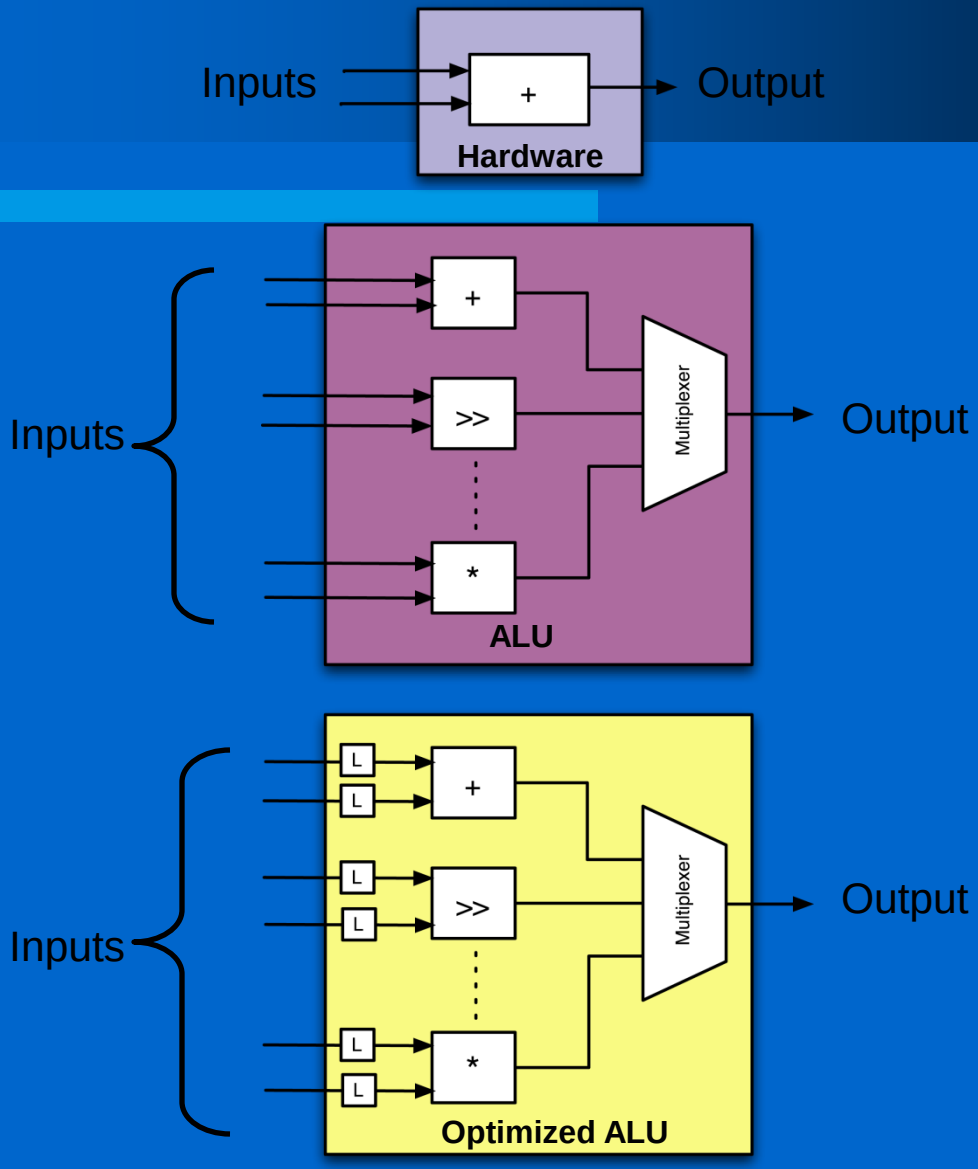
Domain specific fabric

- The fabric is comprised of
  - Power-optimized Arithmetic and Logic Units
  - Configurable interconnect

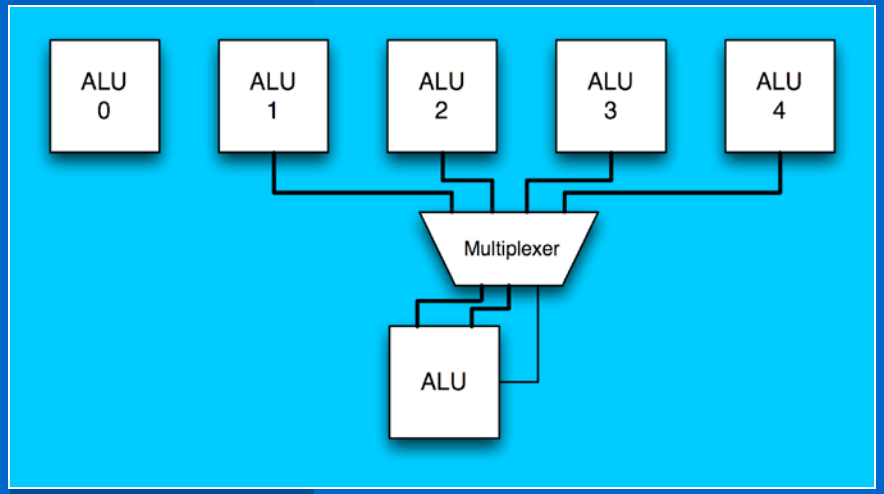


- Characteristics
  - Combinational structure
  - ASIC-like power
  - Programmable

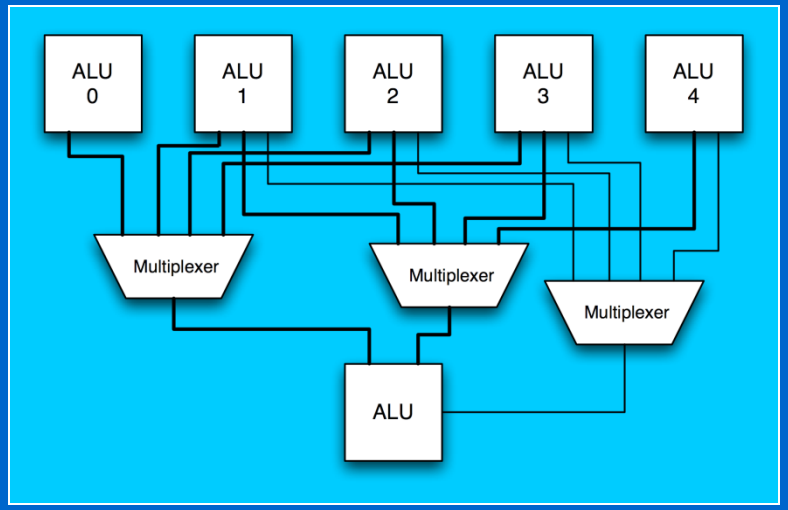
Different architectural implementations of functional units



Interconnect Options



4:1 cardinality interconnect



5:1 cardinality interconnect

Implementation of the fabric

- Implemented the fabric in parameterized VHDL
  - same base VHDL description for the fabric model
  - by varying different parameters, generate different architectural instances

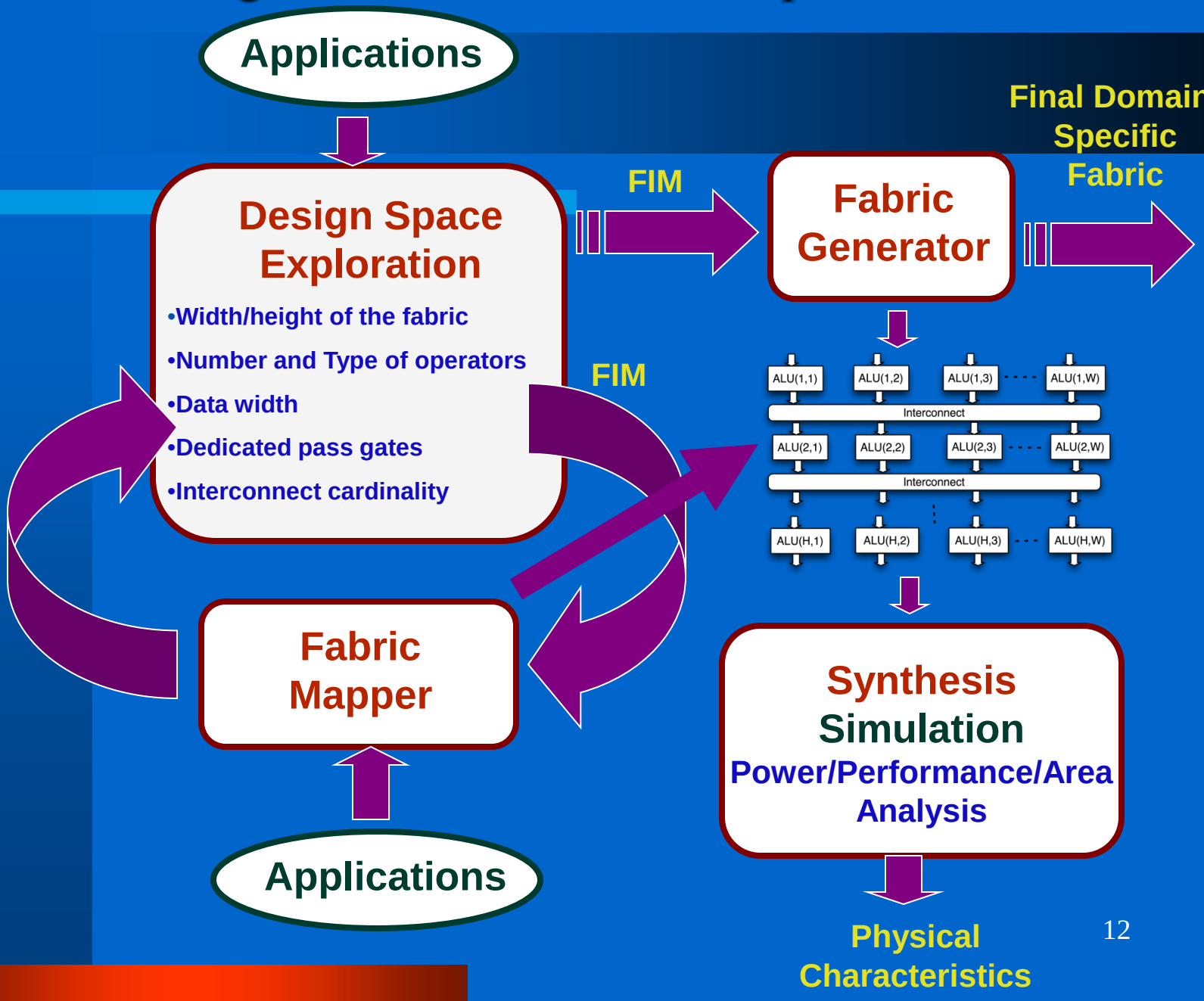
Global Parameters	
Data width	DW={8,16,32}
Fabric Parameters	
Width of the fabric	W
Height of the fabric	H
Arithmetic and Logic Unit Parameters	
Number of Operands	O={3}
Number of Operations	OP={8,10,16, 23}
Interconnect Parameters	
Multiplexer Cardinality	C={2,4,8,16,32}

Design space exploration case studies

- **ALU granularity**
- **Multiplexer cardinality**
- **Dedicated pass gates**
- **Heterogeneous ALUs**

Conclusion: 10 ops per ALU (32-bit) with 8:1 interconnect and 33% dedicated pass gates

Automation of generation of Domain-Specific Fabric



Fabric Instance Model (FIM)

```
<ftudefine
name="alu0“ noop="10111" useic="false">
    <op code="00001"> + </op>
    <op code="00010"> - </op>
    <op code="00011"> * </op>
    <op code="10011"> == </op>
    <op code="00111"> ^ </op>
    <op code="01110"> &gt; </op>
    <op code="10000"> &gt;= </op>
    <op code="01111"> &lt; </op>
    <op code="10001"> &lt;= </op>
    <op code="10010"> != </op>
    <op code="00100"> &amp; </op>
    <op code="00101"> | </op>
    <op code="01001"> &lt;&lt; </op>
    <op code="01011"> &gt;&gt; </op>
    <op code="00000"> pass </op>
    <op code="10100" order="reverse"> pass </op>
    <op code="11111"> mux </op>
    <op code="01000"> ! </op>
</ftudefine>
```

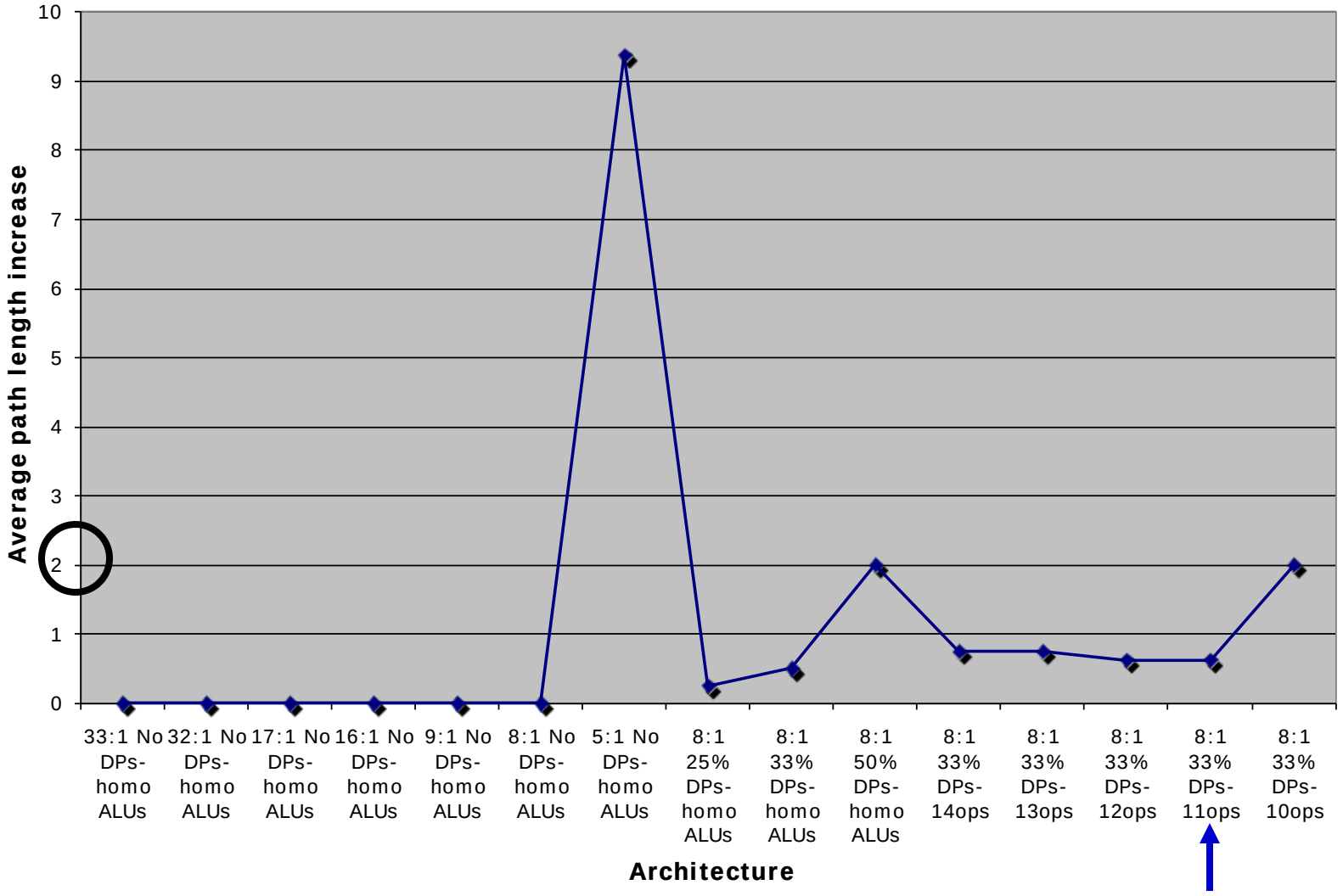
```
<rowpattern repeat="forever">
            <row>
            <ftupattern repeat="forever">
            <FTU type="alu0">

            <operand number="0">

            <range left ="-3" right ="4"/>

            </operand>

            <operand number="1">

            <range left ="-3" right ="4"/>

            </operand>

            <operand number="2">

            <range left ="-3" right ="4"/>

            </operand>
            </FTU>
            </ftupattern>
            </row>
</rowpattern>
```

Energy Consumption

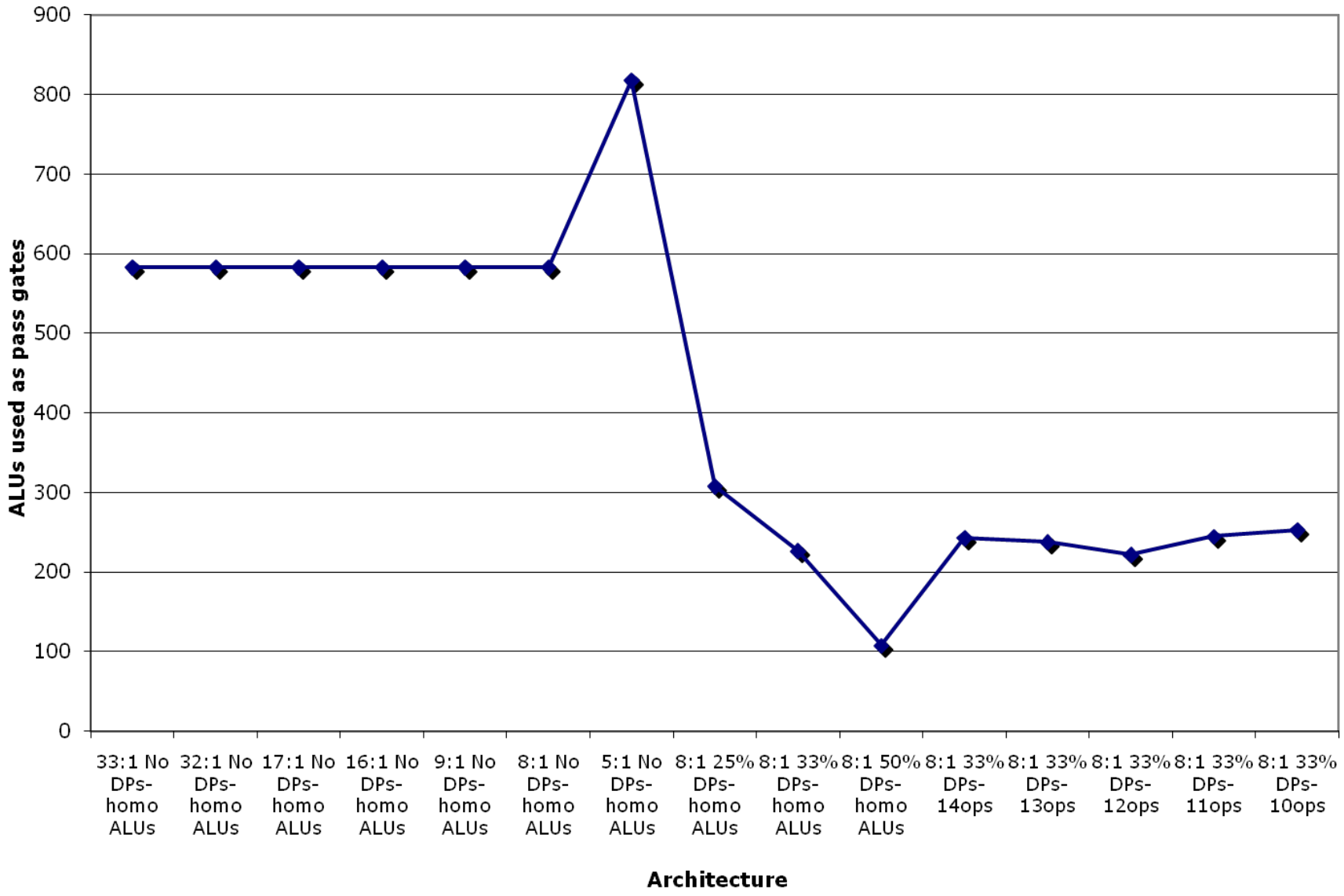
- **Two factors that affect the energy consumption of the device**
  - **Increase in total path length of the mapped application onto the device**
  - **Number of ALUs used as pass gates**

Design Space Exploration

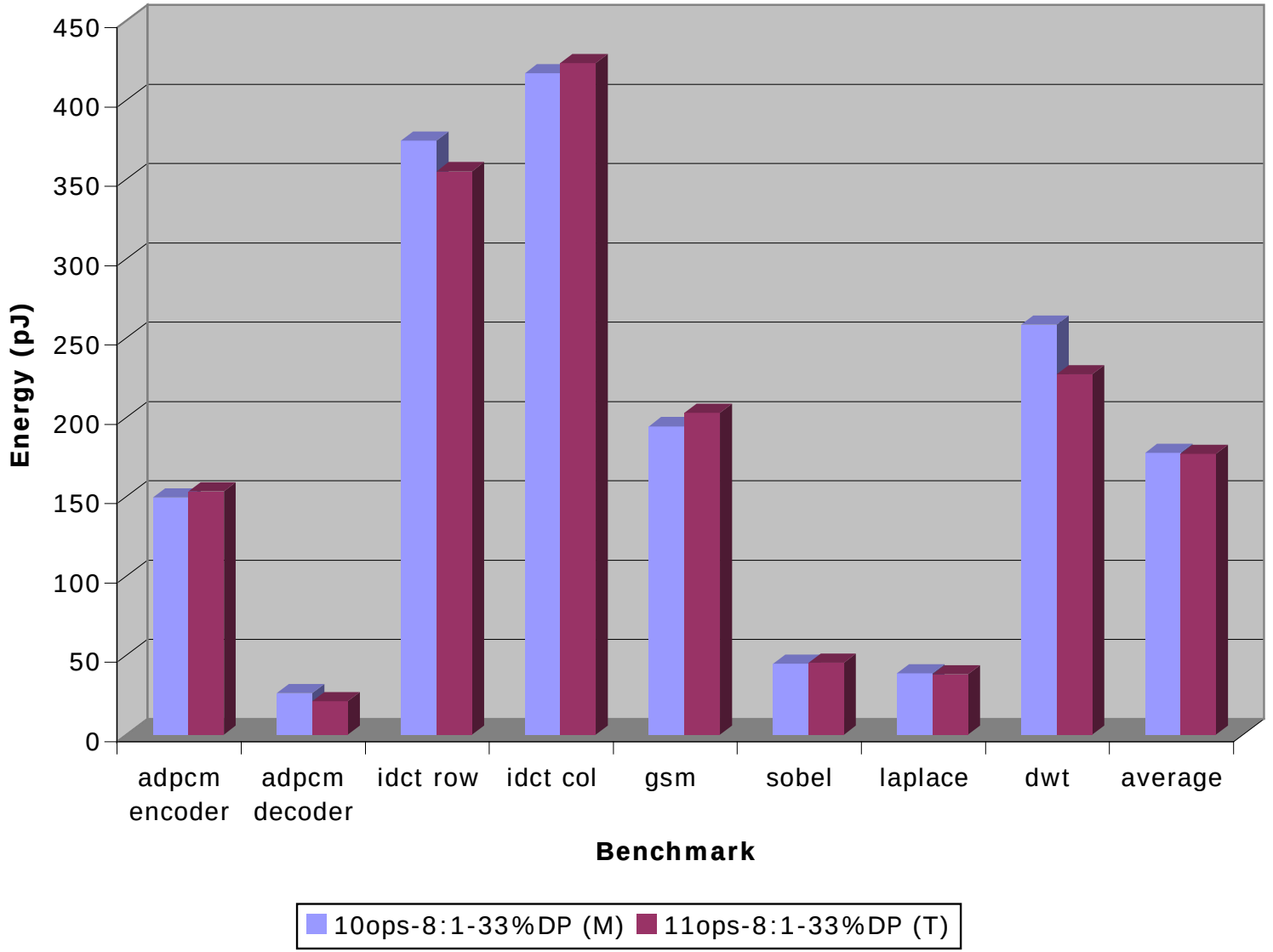
Observation: 11 ops per ALU with 8:1 interconnect & 33% dedicated pass gates is the best candidate



Design Space Exploration

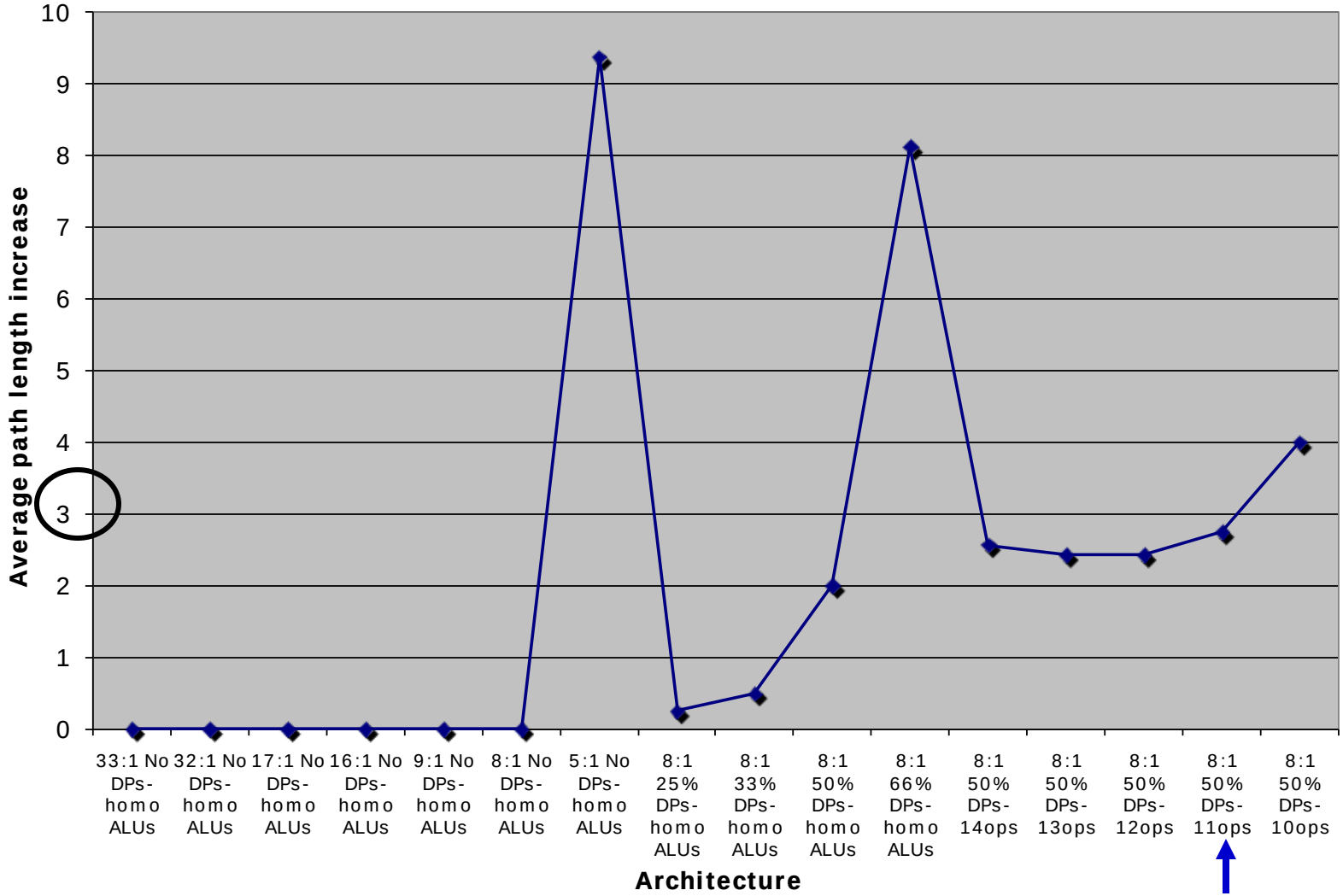


Comparison of manual and tool DSE results

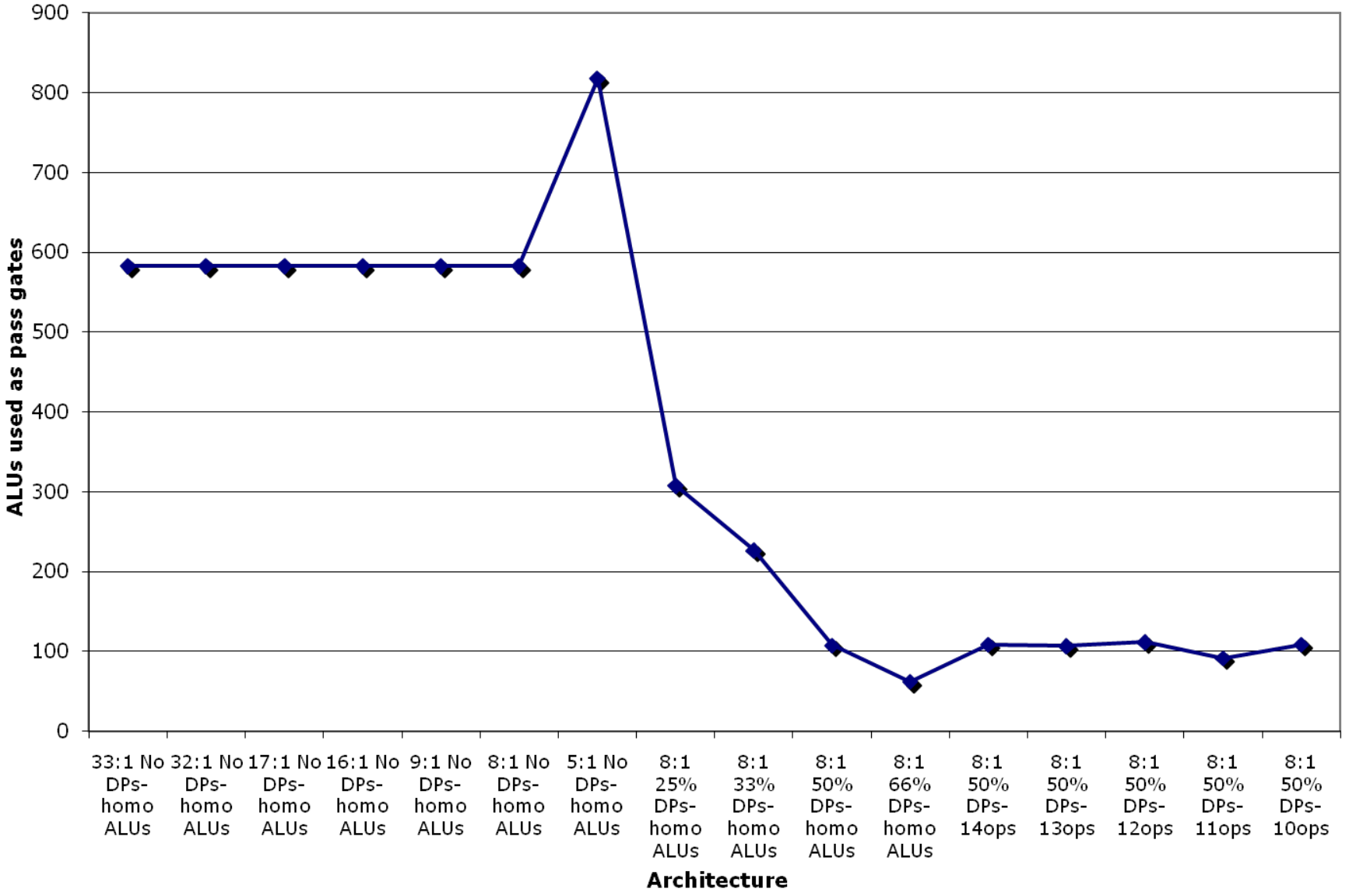


Design Space Exploration

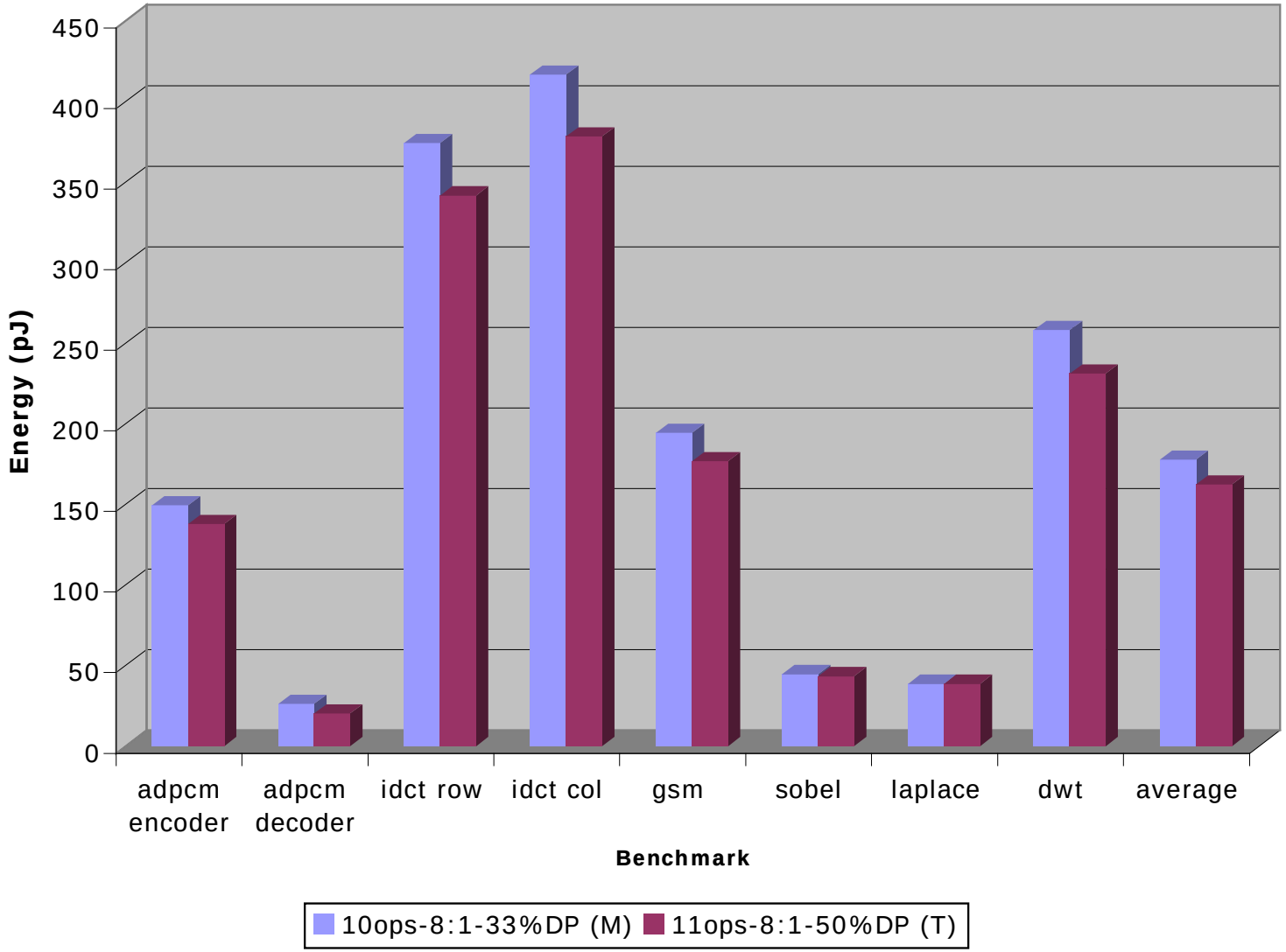
Observation: 11 ops per ALU with 8:1 interconnect & 50% dedicated pass gates is the best candidate



Design Space Exploration

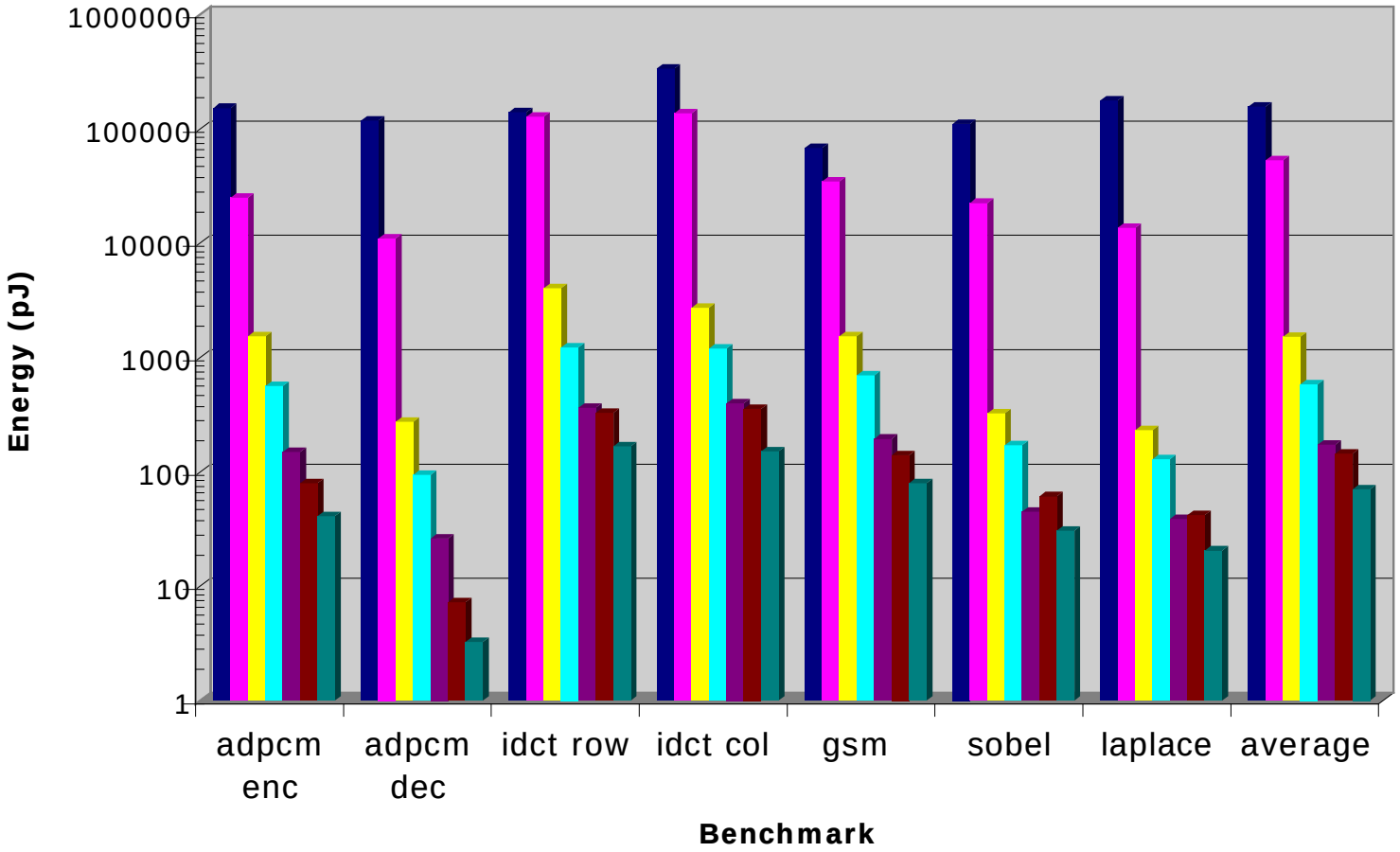


Comparison of manual and tool DSE results



Reconfigurable Fabric Comparison

Observation: Optimized fabric is 3X of ASIC energy



Thank You

Final thoughts and discussion