Will Multi-Core Live Up To It's Promise?

- or -

Fool Me Once…

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The Problem

- Same as it always was…

NOT ENOUGH
PARALLEL SOFTWARE!!

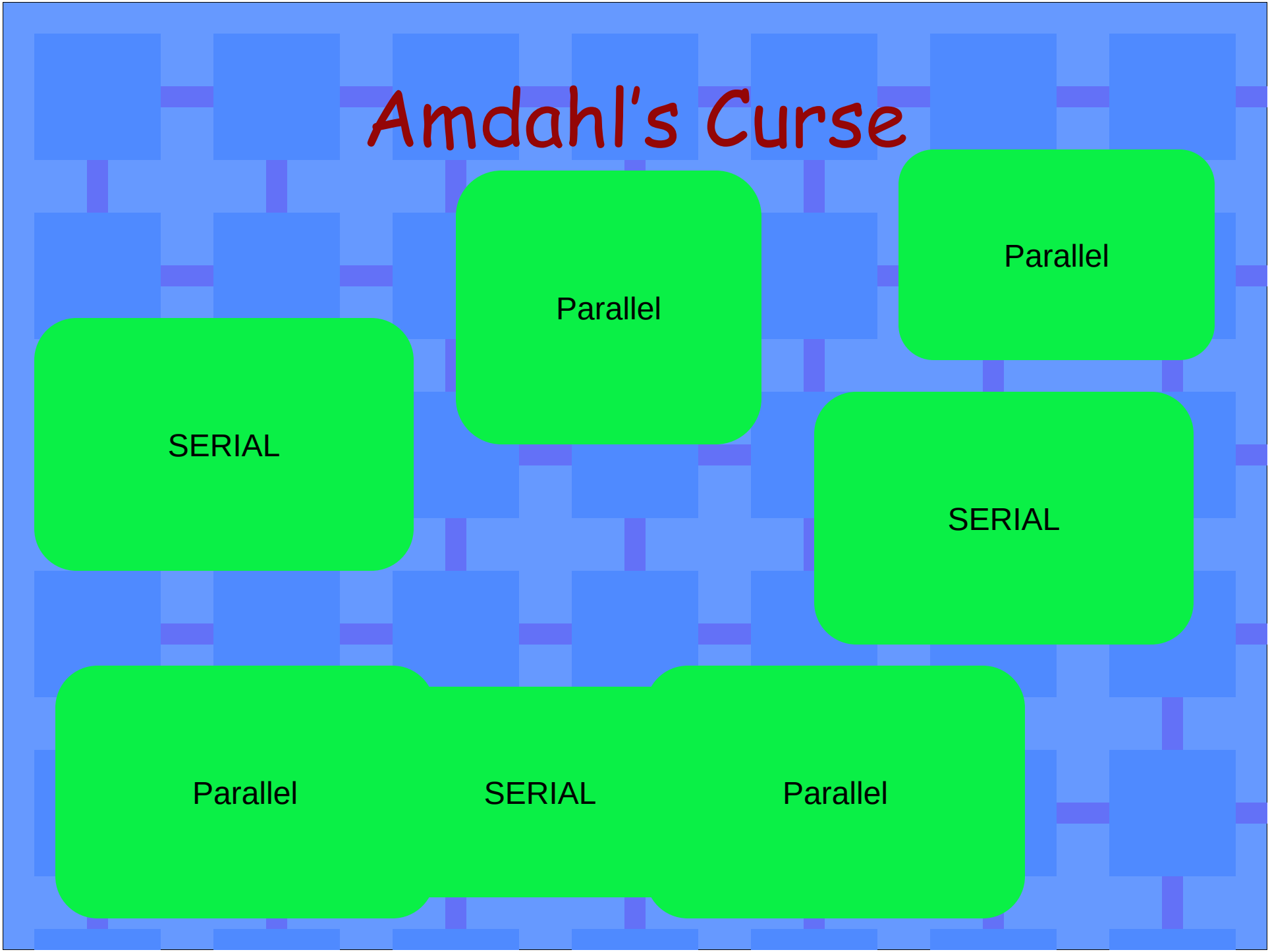
Root Causes

- Parallel programming is hard (parallel code isn't being produced)
- Compilers too conservative (serial code remains serial)

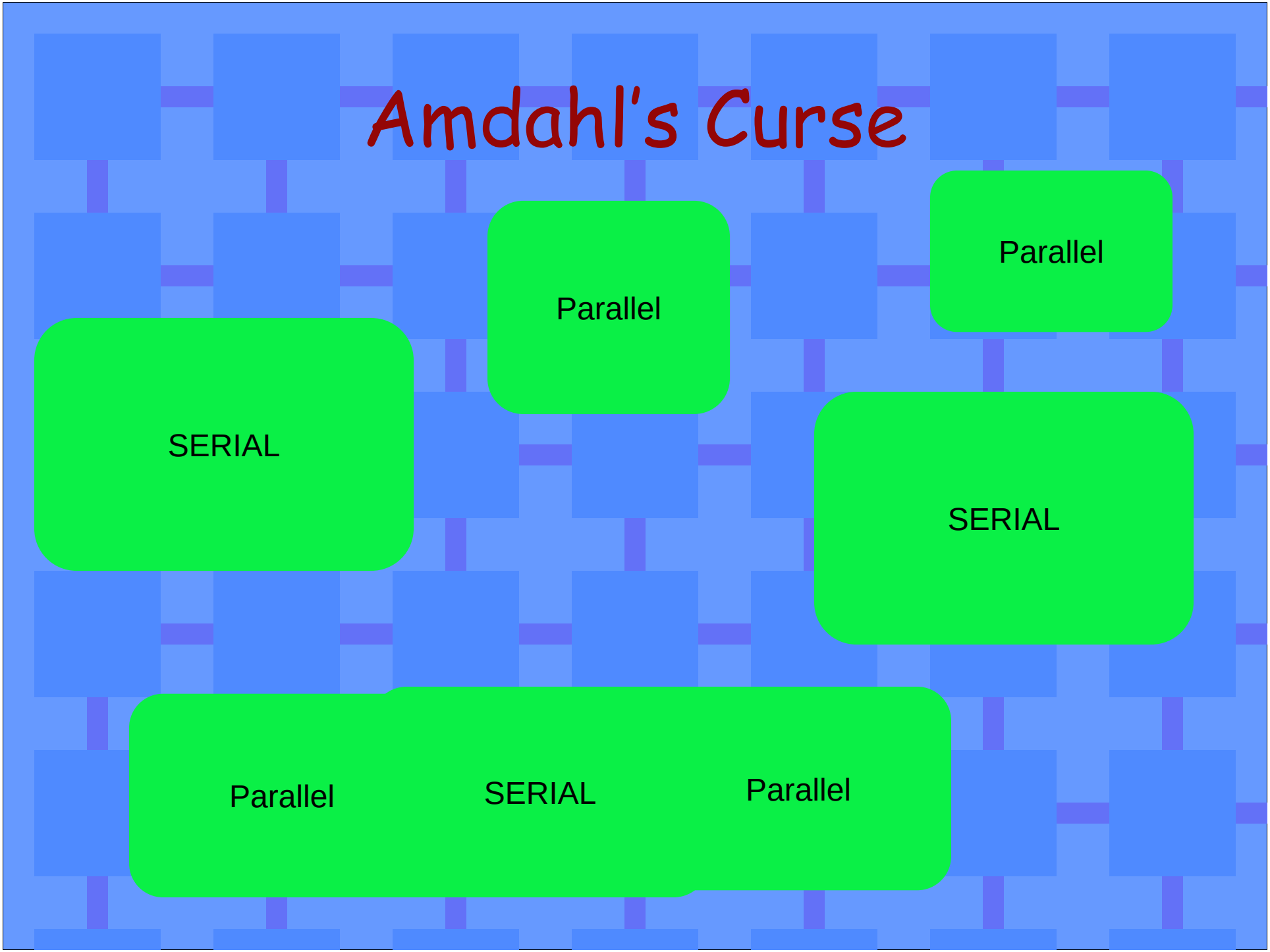
Root Causes

- Amdahl's Curse

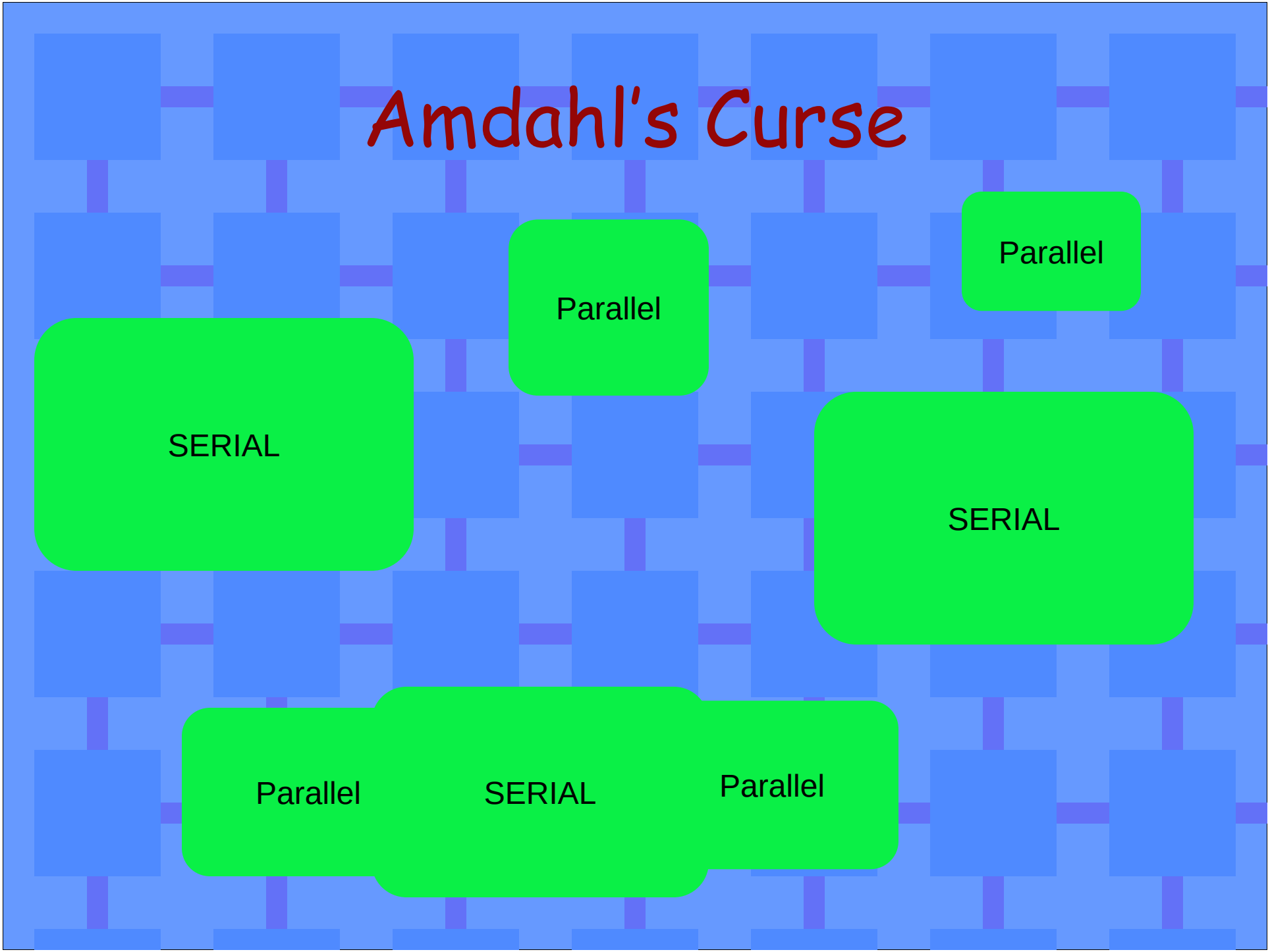
Amdahl's Curse



Amdahl's Curse



Amdahl's Curse



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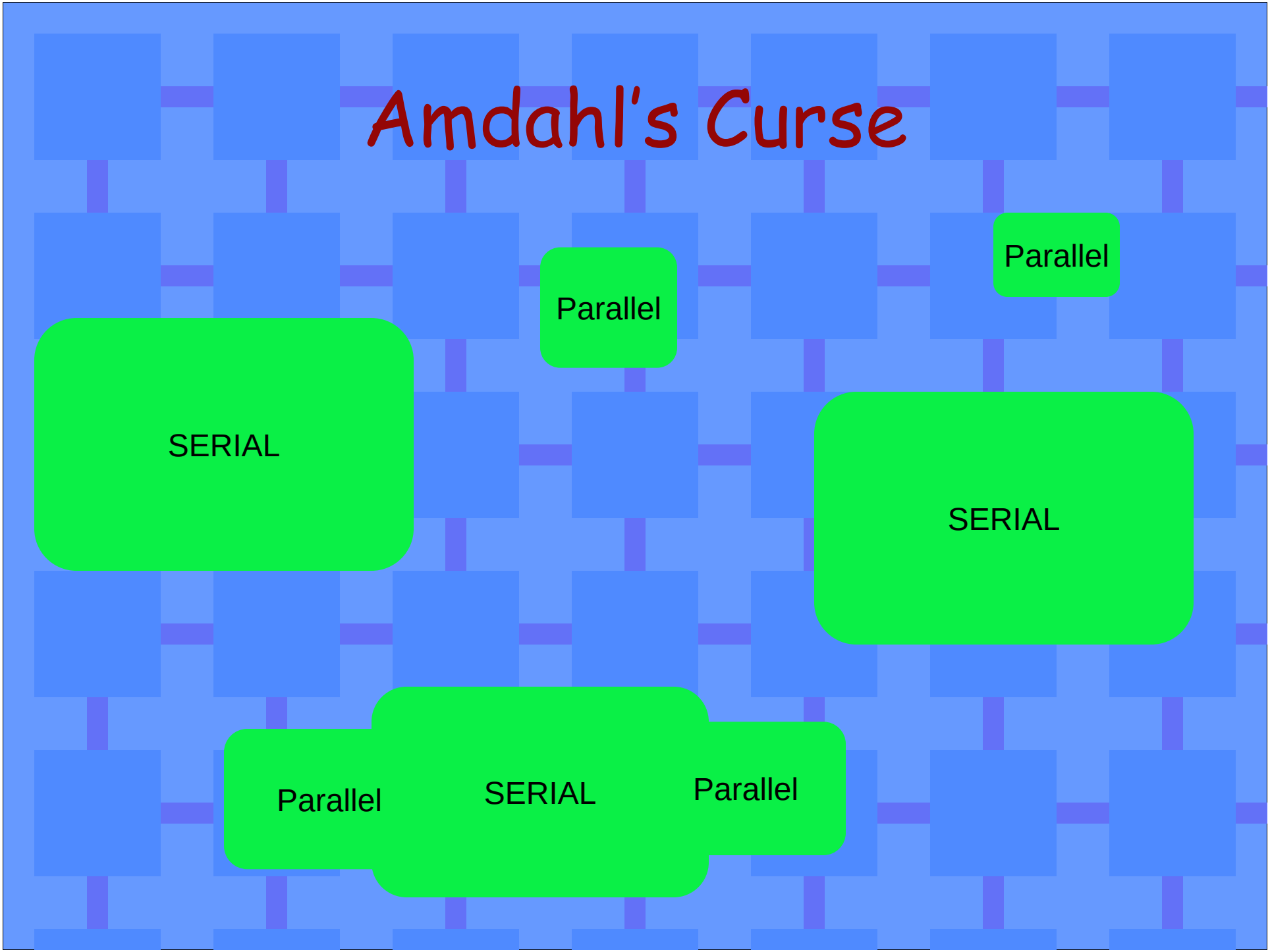

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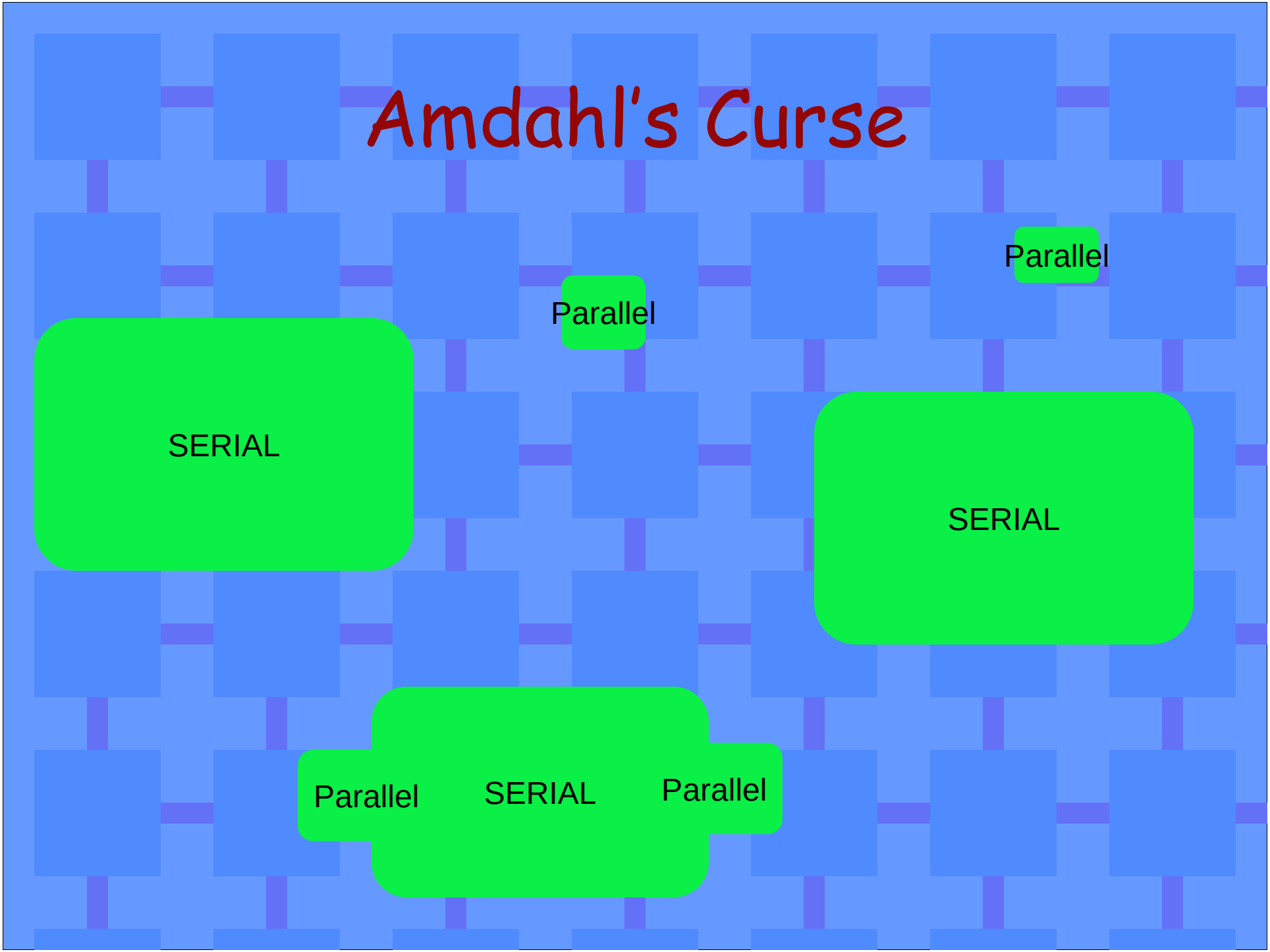


So…..

- None of these root causes have changed!

Causes for Hope

- RISC vs CISC revisited
- The horse and the cart
- Your children and the typewriter
- Not your father's multiprocessor
- It ain't over til Amdahl says it's over

RISC vs CISC revisited

- The RISC vs CISC battle was the major war of the 80s and 90s
- Who won?

The horse and the cart

- The cart always comes after the horse
- The software always comes after the hardware

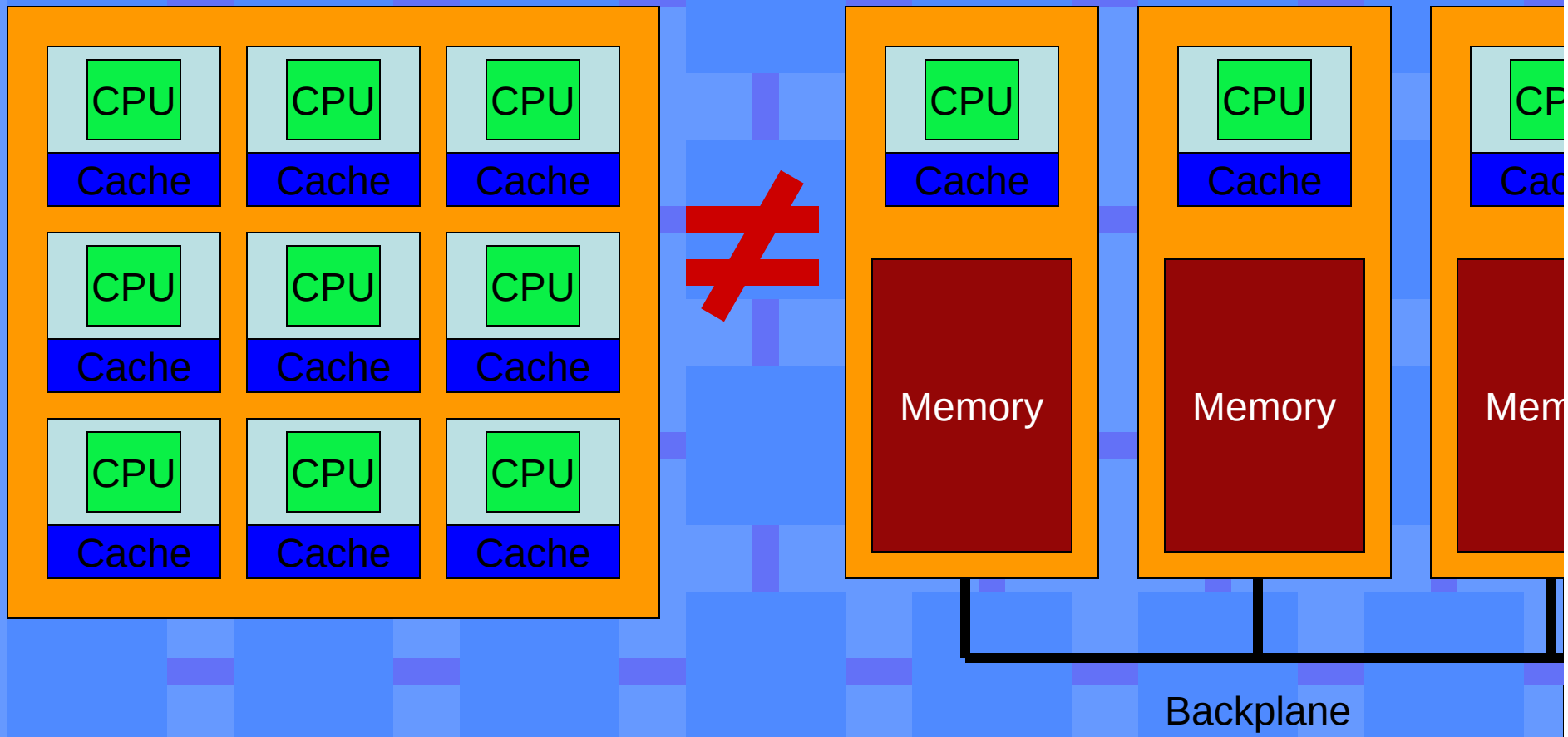
- Parallel hardware has been around for a long time
- But it was never pervasive

The children and the typewriter

- The next generation of programmers will be "born parallel".
- They won't know a uniprocessor from a typewriter or a rotary phone.

- Yes, we think parallel programming is hard.
  - But our parents can't program the VCR/DVR
  - And I can't set the speed dial on my cell phone

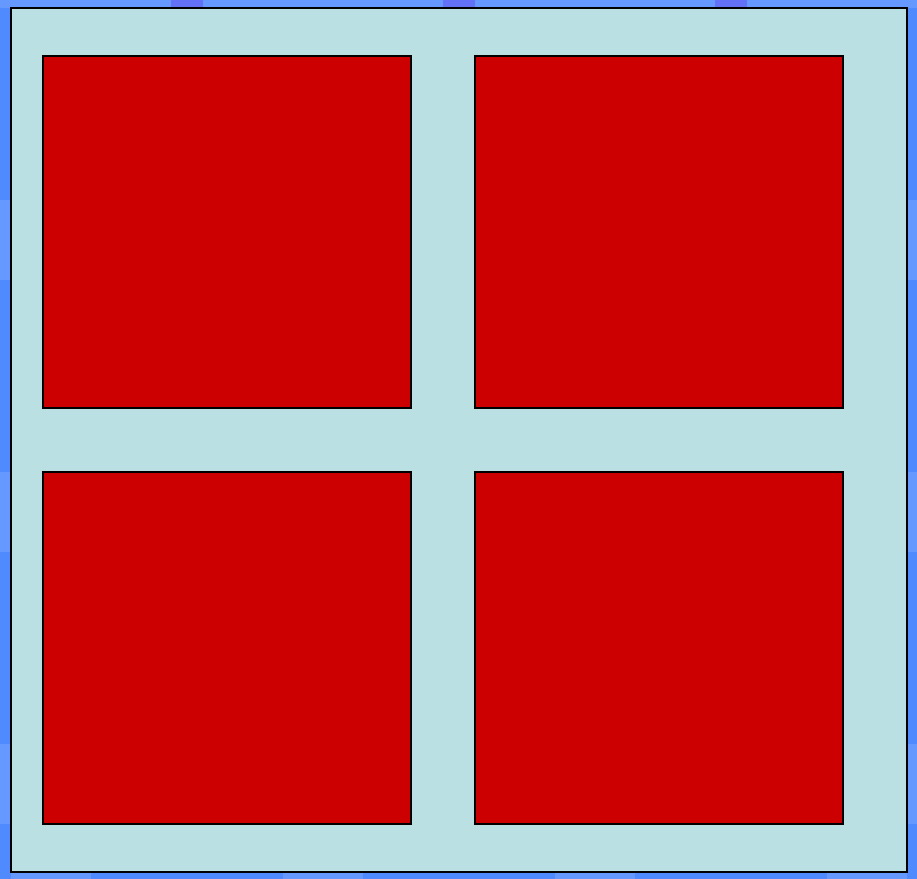
Not Your Father's Multiprocessor



Not Your Father's Multiprocessor

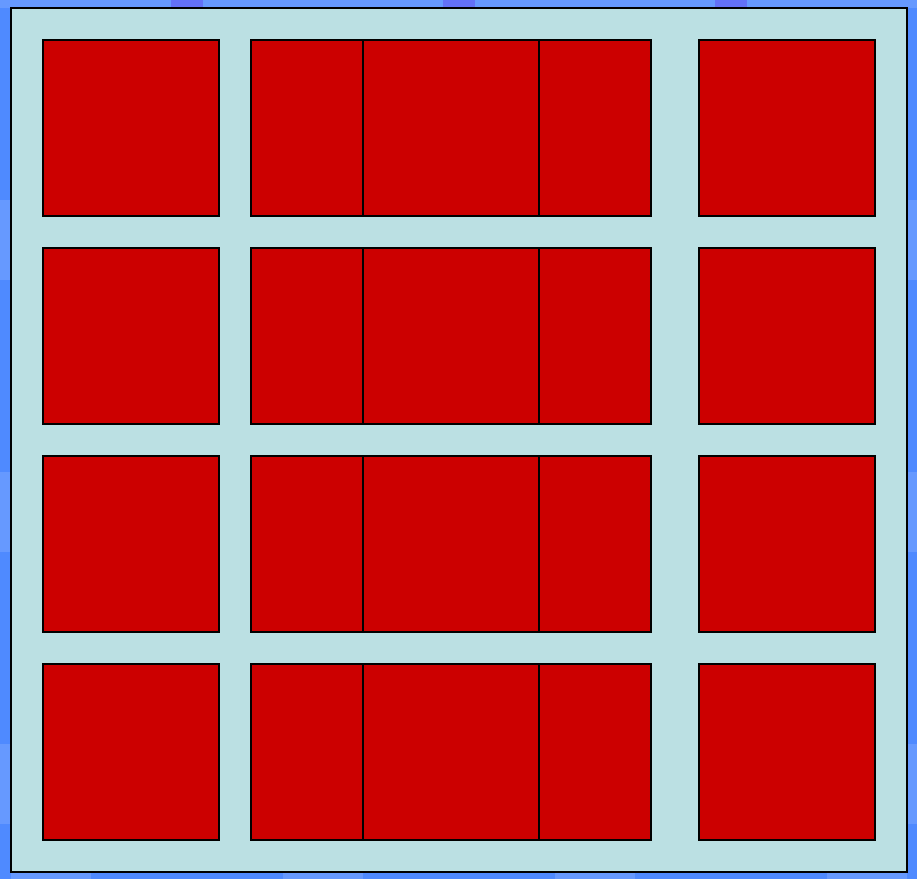
- Communication latencies significantly reduced
  - Threshold for parallelism *potentially* much lower.
- Lots of on-chip cache memory
- New architectural opportunities!
  - Holistic design

Multicore Opportunities



- Heterogeneous Multicore Architectures

Multicore Opportunities

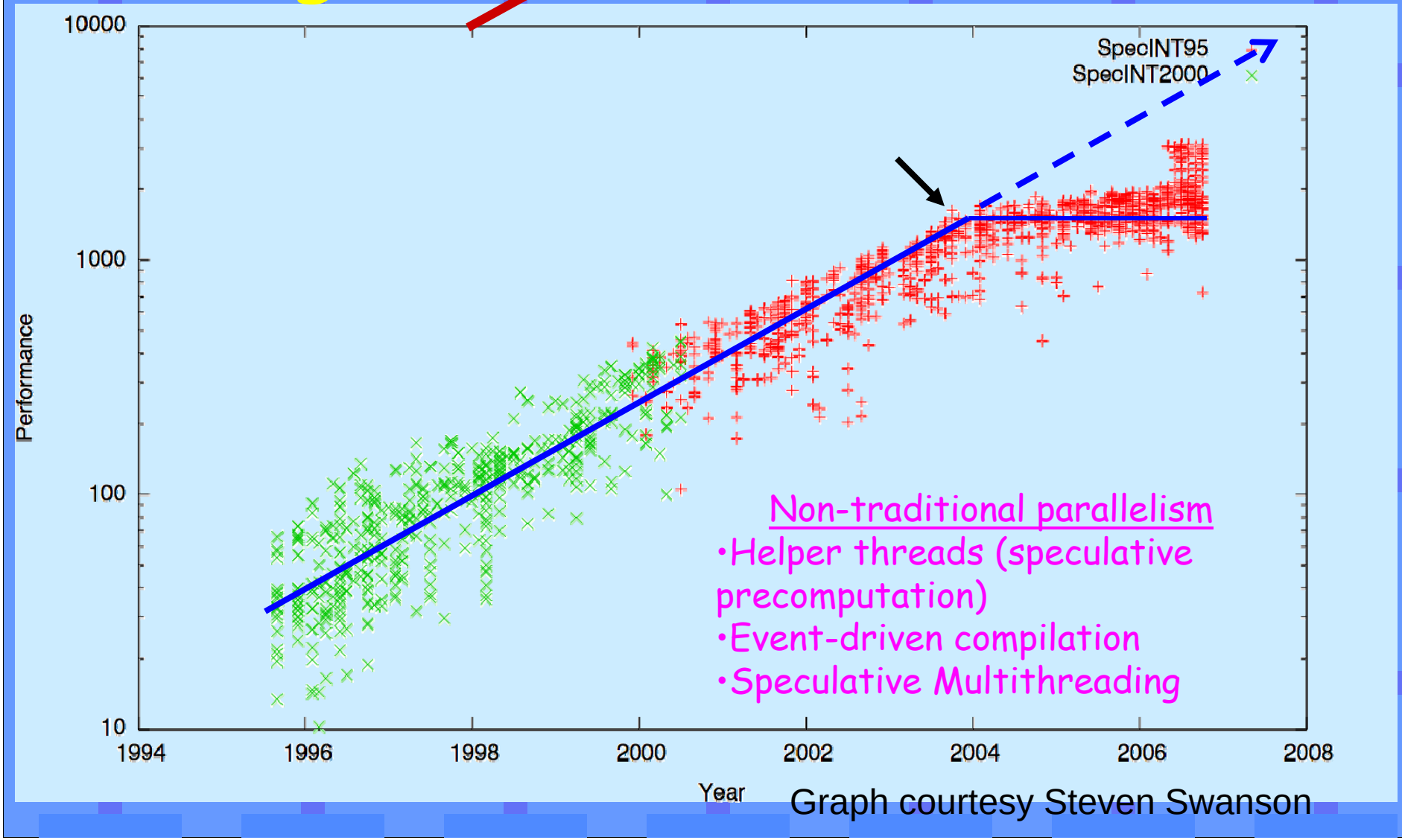


- Conjoined Cores

It ain't over til Amdahl says it's over

Don't give up on single-thread performance yet!

~~core~~ Single-thread Performance



Graph courtesy Steven Swanson

In case no one else said it…

- Need new parallel languages and language support
- Need new compilers
- Need programmer support tools that make analyzing and debugging parallel code as easy as serial code is now.
- Need new architectures that lower the parallelism threshold even lower
- Need more flexible architectures that exploit whatever parallelism is there or not there